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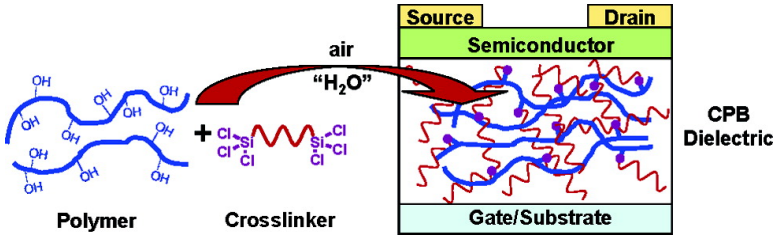

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Low-Voltage Organic Field-Effect Transistors and Inverters Enabled by Ultrathin Cross-Linked Polymers as Gate Dielectrics

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Abstract: The quest for high-performance organic thin-film transistor (OTFT) gate dielectrics is of intense current interest. Beyond having excellent insulating properties, such materials must meet other stringent requirements for optimum OTFT function: efficient low-temperature solution fabrication, mechanical flexibility, and compatibility with diverse gate materials and organic semiconductors. The OTFTs should function at low biases to minimize power consumption, hence the dielectric must exhibit large gate capacitance. We report the realization of new spin-coatable, ultrathin (<20 nm) cross-linked polymer blends exhibiting excellent insulating properties (leakage current densities $\sim 10^{-8}$ Acm^{-2}), large capacitances (up to $\sim$ 300 nF cm^{-2}), and enabling low-voltage OTFT functions. These dielectrics exhibit good uniformity over areas $\sim$150 cm^2, are insoluble in common solvents, can be patterned using standard microelectronic etching methodologies, and adhere to/are compatible with n$^+$-Si, ITO, and Al gates, and with a wide range of p- and n-type semiconductors. Using these dielectrics, complementary invertors have been fabricated which function at 2 V.

Introduction

Organic thin-film transistor (OTFT)-based electronics performing simple operations/functions offer unique attractions compared to traditional inorganics,[1] including flexibility, lightweight, and inexpensive large-area coverage and integration.[2−6] Although speed may be modest versus Si- and inorganic-based circuits, the aforementioned characteristics make OTFT-based electronics attractive for diverse new applications.[7−11] To achieve these goals, the OTFT semiconductor and dielectric components (Figure 1) should ideally be fabricable via high-throughput, low-temperature solution-processing methods such as spin-coating, casting, or printing.[12−15] In a top-contact TFT (Figure 1), source and drain electrodes (typically 50 nm) are defined on top of the organic semiconductor whereas in a typical bottom-contact device (not shown) electrodes are patterned on the dielectric layer before depositing the semiconductor layer (typically 50 nm). The insulating layer is spin-coated on top of the gate substrate. In both top- and bottom-contact configurations, current flow between source and drain electrodes (I_{DS}) on application of a drain-source bias (V_{DS}) is modulated by bias applied between gate and source electrodes (V_G). When $V_G = 0$, I_{DS} is minimal and the device is in the "off" state. When $V_G \neq 0$ is applied, the device turns "on", and charge carriers are accumulated at the semiconductor-dielectric interface, resulting in a gate-controlled I_{DS}. Principal TFT figures-of-merit include field-effect mobility (μ) and current on/off ratio (I_{on}:I_{off}), defining average charge carrier drift velocity and drain-source current ratio between "on" and "off" states, respectively. I_{DS} in saturation ($V_{DS} > V_G$) is then expressed by $I_{DS} = W/2L\ \mu C_i[V_G - V_T]^2$ (eq 1), where L (here, 100 μm) and W (here, 5 mm) are the TFT channel length and width, respectively, V_T the threshold voltage, and C_i the insulator capacitance per unit area expressed by $C_i = \epsilon_0\ k/d$ (eq 2 where k is the dielectric constant, ϵ_0 the vacuum permittivity, and d the insulator thickness). Note that for a given device geometry and semiconductor, equivalent

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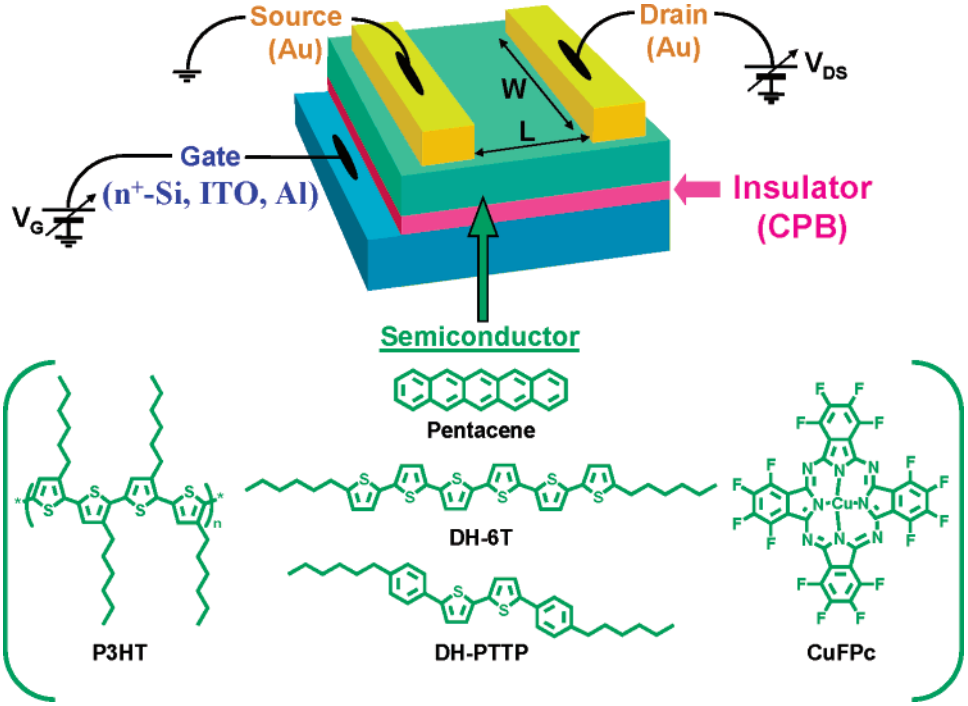

Figure 1. Schematic of a top-contact OTFT and structures of organic semiconductors employed in this study. In the present study, the insulating layer (CPB, 10−20 nm, see Figure 2 for structure) is spin-coated on top of the gate substrate.

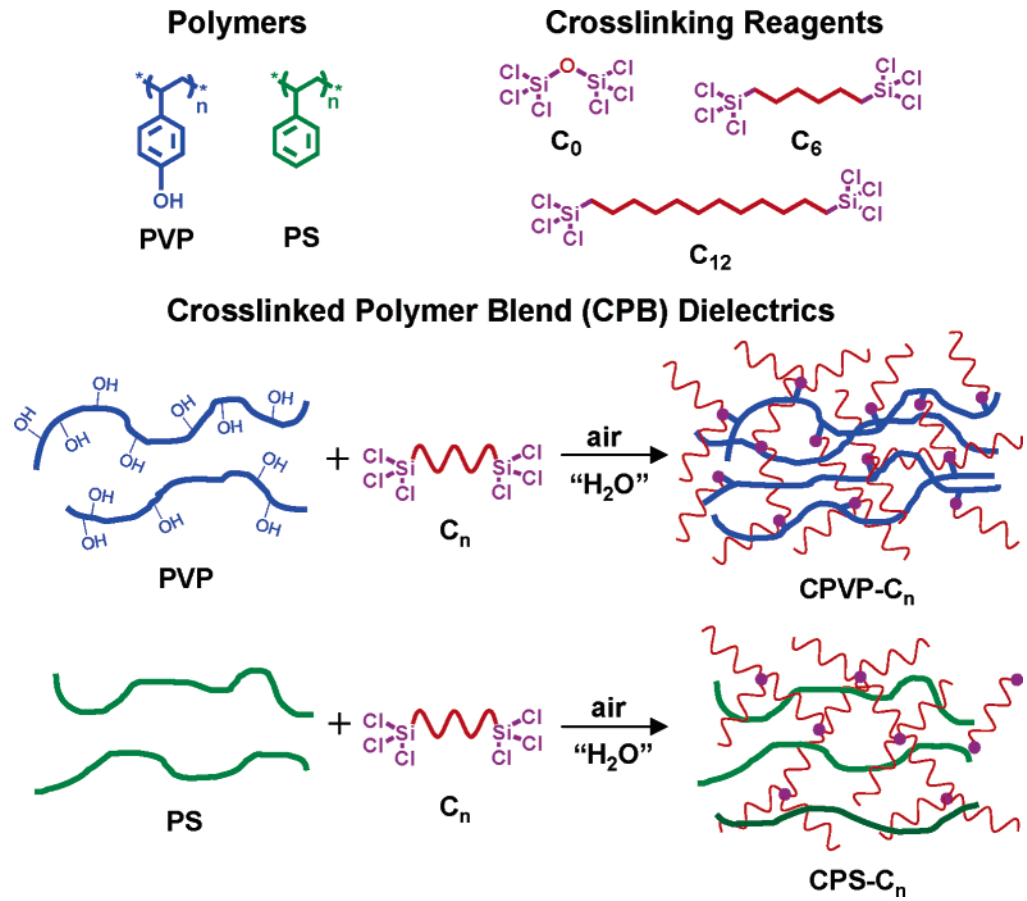

Figure 2. Chemical structures of the polymer and siloxane cross-linkers employed and the CPB dielectric fabrication process.

current gains (I_{DS}) can be achieved at lower operating biases by increasing C_i.

Considerable research has targeted solution-processable organic semiconductor development, with recent impressive progress.[16−25] However, the resulting OTFTs are generally limited by high operating voltages, typically ≫10 V, reflecting the intrinsic low carrier mobilities of the semiconductors and the limitations of the gate dielectrics (typically thick SiO_2 or

polymer films).[26] From eqs 1 and 2 note that operating bias reduction, in a manner similar to increasing the semiconductor mobility, can be achieved by increasing the dielectric constant (k) or decreasing the thickness (d) of the gate dielectric. An increase of the k/d ratio is also essential for efficient device scalability, a prerequisite to improving frequency and low-power TFT operation.[1] One approach to reducing OTFT operating voltages is to employ relatively thick, conventional high-dielectric constant oxide films,[27−31] however, typical vapor-phase deposition processes (sputtering) risk damaging organic components and yielding poor mechanical properties on flexible substrates. Furthermore, ultrathin inorganic insulators are typically electrically "leaky", rendering them incompatible with low-mobility semiconductors. Alternatively, ultrathin, self-assembled organic mono-[32,33] and multilayer[34] dielectrics show promise, however, pathways for integration into large-volume coating processes are less obvious.

Gate insulator materials exhibiting greatest potential for OTFTs are polymers due to their ready processability from solution.[35−40] Thus, PVP, PMMA, and polyimides have been investigated with a limited variety of organic semiconductors, however the resulting OTFTs operate at relatively high voltages. This reflects the substantial insulator thicknesses (usually $\gg$0.3 μm) required to reduce gate leakage currents to acceptable levels, thereby affording low capacitance metrics (typically $\ll$ 20 nF cm^{-2}). An innovative alternative recently reported by Bao, et al. grows polymeric insulators in situ on the gate surface, and offers, in principle, tunable thickness control.[41] However, reported capacitances are again modest ($\sim$3 nF cm^{-2}) for low-voltage OTFT applications. Recently, the Cambridge group described the thinnest polymer dielectrics achieved to date (50−100 nm) for top-gate polymer-based OTFTs, which operate at relatively low voltages ($\sim$10 V) with a triarylamine semiconductor.[42] This represents a significant advance, however the polymerization/annealing temperatures are too high (230−290 °C) for typical polymeric substrates, and reported device *I-V* saturation characteristics not ideal. In this report, we demonstrate a new low temperature approach which realizes high-quality cross-linked OTFT polymer dielectrics from straightforward polymer/molecular precursors. The cross-linking (insolubility) ensures that subsequent device layers can be spin-coated or printed on top without dissolution of the dielectric and that the dielectric is covalently grafted to the surface of typical gate materials. To our knowledge, these 10−20 nm-thick polymeric insulators exhibit the largest k/d ratios and lowest leakage currents (considering the thickness range) achieved to date for conventional and cross-linked polymer gate OTFTs, and afford devices with extremely low operating biases. Moreover, we show here that these dielectrics are electrically uniform over large areas, are compatible with both bottom and top contact device geometries, can be readily patterned for vertical interconnects, can be used to fabricate complementary inverters, and that this approach is applicable to diverse gate and semiconductor materials.

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Experimental Section

Reagents. Poly-4-vinylphenol (**PVP**; M_w = 8K) and polystyrene (**PS**; M_w = 1M) (Aldrich) were used without further purification. Hexachlorodisiloxane and 1,6-bis(trichlorosilyl)-hexane (Gelest) were purified by distillation under inert atmosphere. The reagent 1,12-bis(trichlorosilyl)dodecane was synthesized as follows. *1,12-bis(trichlorosilyl)dodecane.* Trichlorosilane (25.14, 19.0 mL, 185.6 mmol) was added to a solution of 1,11-dodecadiene (TCI, 3.85 g, 23.2 mmol) and a few crystals of $H_2PtCl_6 \times H_2O$ (Aldrich) under nitrogen. After stirring overnight at room temperature, the solution was filtered and the excess of $HSiCl_3$ and solvent were removed under dynamic vacuum leaving a yellow oil which was used without additional purification. ^{1}H NMR ($CDCl_3$) δ 1.63−1.56 (m, 4H), 1,43−1.40 (m, 8H), 1.31−1.28 (m, 12H). HRMS (EI, 70 eV): found *m*/*z* 433.9538 (M^+), calcd for $C_{12}H_{24}Cl_6Si_2$, 433.9548.

Materials. n^+-Si wafers (Montco Silicon Tech) and ITO-coated glass substrates (≤30 Ω/sq, Thin Film Devices) were cleaned according to standard procedures. Aluminum substrates were cut from commercially available Al foil (Reynolds Consumer Products). All of the organic semiconductors were commercially available or prepared by published procedures.[23]

Film Fabrication and Characterization. For **CPVP-C**$_n$ fabrication, **PVP** (4 mg/mL in anhydrous THF) was mixed with the trichlorosilyl reagent (4 mg/mL in anhydrous THF) in a 1:1 volume ratio, spin-coated onto substrates at 5000 rpm, and then cured in a vacuum oven at 100−110 °C for 10−15 min. For **CPS-C**$_n$ fabrication, **PS** (7 mg/mL in anhydrous toluene) was mixed with the trichlorosilyl reagent (7 mg/mL in anhydrous toluene) in a 1:1 volume ratio, diluted with 2 parts of toluene, spin-coated onto substrates at 4000 rpm, and then cured in vacuo at 100−110 °C overnight. **PVP**-only and **PS**-only films were spin-coated from 20 mg/mL THF and toluene solutions, respectively, at 2500 rpm, and were dried in vacuo at ∼100−110 °C for ∼2 h.

The morphologies of all thin films were evaluated by atomic force microscopy (AFM) using a Nanoscope III microscope with A and D scanners (Digital Instruments, Inc.). All images were recorded under ambient conditions in the contact mode with Si_3N_4 cantilevers having pyramidal tips with 70° cone angles and 20−50 nm radii of curvature. No attempt was made to account for tip convolution. The cantilever had a force constant of 0.12 N/m. The images were obtained using the height mode with a total force of 20−60 nN and a scan rate of ∼10 Hz. The same image was scanned at least three times to ensure the reproducibility as well as by scanning different area sizes (i.e., higher or lower magnifications) to verify image consistency. All the RMS surface-roughness values are reported over an area of 25 μm^2. Thicknesses of all organic thin films were measured using a Tencor P-10 surface profiler.

Electrical Measurements. OTFTs were fabricated and evaluated as described previously.[20] Gold electrodes for OTFT/MIS/MIM devices were vacuum-deposited through shadow masks at (3−4) × 10^{-6} Torr (1000 Å, 0.2−0.5 Å/s). OTFT measurements were carried out in air using a Keithly 6430 subfemtoammeter and a Keithly 2400 source meter, operated by a local Labview program and GPIB communication. Triaxial and/or coaxial shielding was incorporated into Signaton probe stations to minimize the noise level. A digital capacitance meter (Model 3000, GLK Instruments) and impedance/gain-phase analyzer (SI 1260, Solartron Analytical) were used for capacitance measurements.

Table 1. Summary of Dielectric (10 kHz) and Film Properties of Polymeric Dielectrics

dielectric	film thickness[a] (nm)	RMS roughness[a] (nm)	C_i[b] (nF cm^{-2})	ϵ[c]
CPVP−C$_0$	18	6−8	305	6.2
CPVP−C$_6$	18	2	300	6.1
CPVP−C$_{12}$	20	6	289	6.5
CPS−C$_0$	12	8−10	220	3.0
CPS−C$_6$	10	1.5	218	2.5
CPS−C$_{12}$	13	5	200	2.9
PVP	133	6	42	6.4
PS	122	2	19	2.6
SiO$_2$[d]	300	2	11	3.9[e]

[a] Measured on n^+-Si substrates (substrate rms roughness ≈ 0.5 nm). [b] Measured on MIS structure. [c] Calculated from eq 2. [d] From commercial source. [e] Literature value [ref 28].

Results and Discussion

Dielectric Synthesis and Characterization. The new cross-linked polymer blend (CPB) materials (Figure 2) are prepared by spin-coating of a solution of an appropriate polymer and α,ω-bis(trichlorosilyl) cross-linking reagent using procedures described in the Experimental, resulting in films with 10−20 nm thicknesses as established by profilometry. All operations are performed in air in a simple fume hood. The films are next cured at ∼110−115 °C for times dependent on the spin-coating solvent (e.g., 10−15 min for THF). Under these conditions, the chlorosilane hydrolysis/condensation/cross-linking process occurs within seconds in ambient. Note that we have not attempted to fully optimize processing at this stage. Films of greater thicknesses if required (vide infra), can be obtained by varying the processing conditions or by multiple spin-on depositions since the cross-linked CPBs are insoluble in the mother solutions at all stages of curing. To assess the influence of CPB structure (Figure 2) and the effects of polymer microstructure and cross-linker on film properties, two polymers, poly-4-vinylphenol (**PVP**) and polystyrene (**PS**), and three cross-linkers, hexachlorodisiloxane (**C$_0$**), 1,6-bis(trichlorosilyl)hexane (**C$_6$**), and 1,12-bis(trichlorosilyl)dodecane (**C$_{12}$**), were investigated. The cross-linked films, **CPVP-C**$_n$ and **CPS-C**$_n$, are structurally quite different. In **CPVP-C**$_n$, **PVP** chains are σ-bonded to a siloxane network whereas for **CPS-C**$_n$, **PS** chains are simply embedded as guests in a cross-linked matrix. It will be seen that this affords materials with substantially different properties versus those of neat **PVP** and **PS** films of similar/greater thicknesses, and which are characterized here by atomic force microscopy (AFM) as well as metal−insulator−metal (MIM) and metal−insulator−semiconductor (MIS) leakage and capacitance measurements. Table 1 collects important metrics for these materials.

AFM images of CPB films reveal that surface morphology is more dependent on cross-linking reagent than on polymer architecture (Figure 3). Since a smooth dielectric-semiconductor interface is essential for efficient transport in the TFT channel,[43,44] AFM data provide important information for initial materials evaluation. The **CPVP-C$_0$** and **CPS-C$_0$** AFM images exhibit very rough surfaces, having large densities of grains and flakes, with a 6−10 nm rms roughness (Figure 3A). In contrast,

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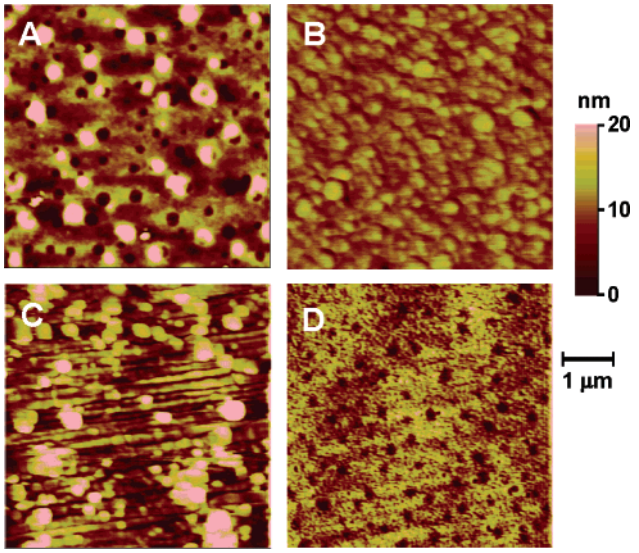

Figure 3. Contact mode AFM images (5 × 5 μm scan area) for evaluation of film morphology and substrate/insulator surface quality. A. **CPVP-C$_0$**. B. **CPVP-C$_6$**. C. Kitchen Al foil. D. Al foil after three consecutive **CPVP-C$_6$** depositions.

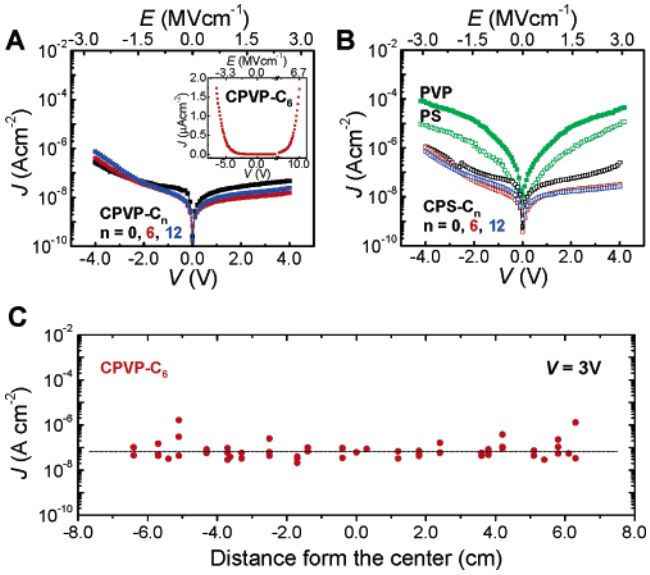

Figure 4. Electrical properties of **CPVP**- (filled symbols) and **CPS**- (empty symbols) **C$_n$** (C$_0$ = black, C$_6$ = red, C$_{12}$ = blue) films versus those of neat **PVP** (green filled symbol)/**PS** (green empty symbol) films. Note that the voltage axis refers to CPB films only. A. Leakage current density J vs voltage plots for **CPVP-C$_n$** [d (nm) = 17 (C$_0$), 14 (C$_6$), 10 (C$_{12}$)] films. **Inset**: Extended plot for a **CPVP-C$_6$** film (13 nm). B. Leakage current density J versus voltage plots for **CPS-C$_n$** [d (nm) = 12 (C$_0$), 11 (C$_6$), 13 (C$_{12}$)], **PVP** (133 nm), and **PS** (122 nm) films. C. Leakage current density J distribution (V = 3.0 V) for a **CPVP-C$_6$** film (~24 nm) over a 130 mm Si wafer.

CPB films cross-linked with **C$_6$** are far smoother, exhibiting an rms roughness of ~1.5−2 nm (Figure 3B), and exhibit no major defects or pinholes. Note that thin/thick neat **PVP** and **PS** films are also very smooth. However, close examination reveals that smooth regions are accompanied by major pinholes which will inevitably compromise dielectric performance. The **CPS-C$_{12}$** films are somewhat rougher than **CPVP-C$_6$** and **CPS-C$_6$**, possibly because the longer **C$_{12}$** chains aggregate in the spin-coating solvents, resulting in grainy cross-linked films. The greater **CPVP-C$_0$** and **CPS-C$_0$** film roughness is probably the combined result of greater **C$_0$** moisture sensitivity, versus α,ω-alkane-linked chlorosilanes (**C$_6$** and **C$_{12}$**), resulting in rapid cross-linking as well as absence of a "flexible" linker between the silyl termini, yielding a less flexible network. Note that **CPVP-C$_6$** and **CPS-C$_6$** also planarize rough substrates such as commercial kitchen Al foil or glass. For example, the rms roughness of commercial Al substrates (Figure 3C), ~11−14 nm, is reduced to ~4−6 nm after depositing a ~60 nm-thick **CPVP-C$_6$** film (Figure 3D).

The dielectric characteristics of the cross-linked dielectric films were next evaluated via quantitative leakage current and capacitance measurements. Figure 4 shows typical current density-electric field (J-E) plots for MIS structures fabricated with CPB and **PVP**/**PS** insulators, demonstrating that these ultrathin cross-linked materials exhibit superior insulating properties vs the corresponding neat polymers of far greater thickness. Leakage current densities for d = 10−20 nm **CPVP-C$_n$** and **CPS-C$_n$** films are $10^{-7} - 10^{-8}$ A cm^{-2} up to $E \approx 2$ MV cm^{-1} (± 3V) compared to $10^{-4} - 10^{-7}$ A cm^{-2} ($E \approx 2$ MV cm^{-1}) for d = 120−130 nm **PVP** and **PS** films. The former metrics are also substantially lower than those of a several hundred nm-thick melamine-cross-linked **PVP** films[36] and comparable to those of μm-thick polymer dielectrics and far thicker oxide films.[35] Furthermore, Figure 4C demonstrates that CPB films of excellent electrical uniformity can be deposited by the present procedure over a 13 cm diameter Si wafer, with average leakage current densities for a **CPVP-C$_6$** film (~24 nm) of 7.8 ± 2.3 × 10^{-8} A cm^{-2} (V = 3 V) when sampling over 60 wafer locations. Furthermore, **CPVP-C$_n$** films strongly adhere to substrates, do not undergo delamination/cracking on substrate bending or solvent treatment (e.g., 30 s sonication in organic solvents) in accord with the highly cross-linked/bonded microstructure. Leakage currents, capacitances, and OTFT characteristics (vide infra) are invariant to ambient and solvent exposure, demonstrating potential for subsequent solution-phase processing/fabrication steps. In contrast, partial delamination or complete dissolution occurs for **CPS-C$_n$** and **PVP** or **PS** films, respectively.

Dielectric Patterning and Capacitance. Despite excellent adhesion and solvent resistance, the **CPVP-C$_n$** films can be conveniently patterned as required for vertical interconnect fabrication using conventional microelectronic lithography and reactive ion etching (RIE) or liquid-phase buffer oxide etching (BOE). As proof-of-concept, Figure 5A shows an image of shadow-mask fabricated Au pads on a **CPVP-C$_6$**/Si substrate. After dielectric removal from the exposed areas (Figure 5B), the resulting patterned MIS structures exhibit leakage current densities comparable to those of unpatterned areas (Figure 5B), demonstrating that RIE/BOE patterning does not alter the quality of the underlying dielectric layer. After subsequent Au removal, the optical image clearly shows the patterned dielectric region, while profilometry and AFM (Figure 5C) demonstrate that the thickness of the dielectric is unchanged. Finally, Au pad deposition in regions where the dielectric layer was removed demonstrate formation of excellent electrical contacts to the bottom (gate) with J increased > 6 orders of magnitude (R < 1 kΩ at 3V) versus those in MIS structures (Figure 5B).

To quantify CPB film capacitances, dielectric constants, and loss factors as a function of frequency ($10^3 - 10^6$ Hz), capacitance-voltage (C_i-V) and capacitance-frequency (C_i-f) measurements were performed on metal−insulator-semiconduc-

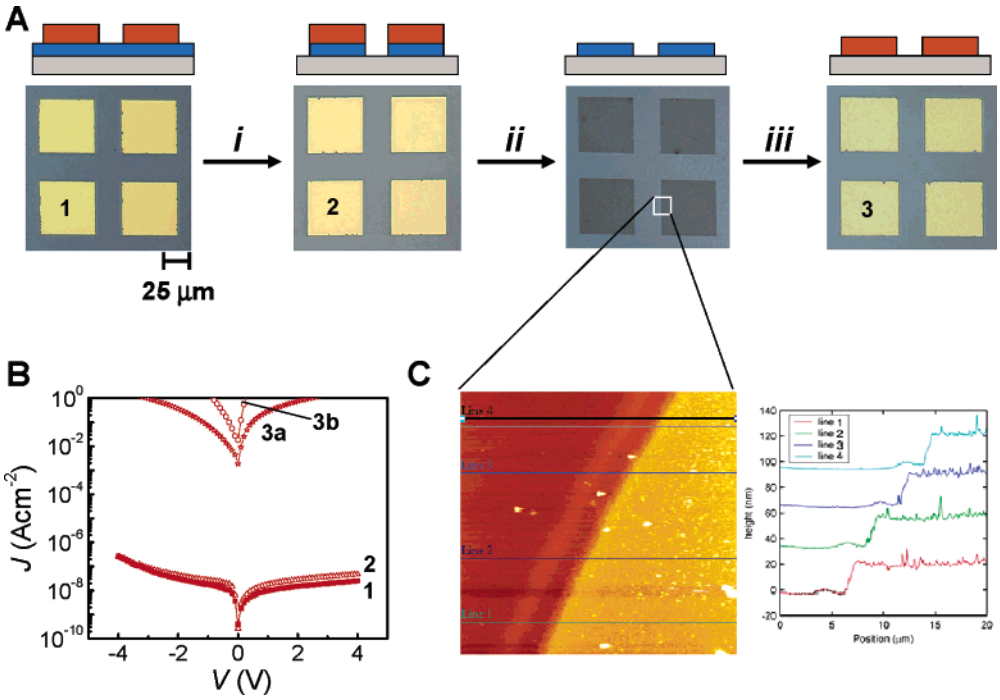

Figure 5. Patterning of **CPVP-C$_6$** films and corresponding film electrical properties. A. Optical micrographs of a series of pads having the cross-sectional structure depicted above the corresponding image [gray = Si substrate; blue = dielectric (23 nm); orange = Au (50 nm)]. Patterning process: (i) Dielectric etching with RIE (5 min) or BOE (30 s); (ii) Au etching with I_2-KI-H_2O (1 min); (iii) RIE or BOE, and then Au deposition. B. Leakage current density recorded on the unpatterned (line 1) and patterned (line 2) dielectric on Si and after dielectric removal with RIE (line 3a) and BOE (line 3b). C. AFM line scans of the dielectric step after patterning.

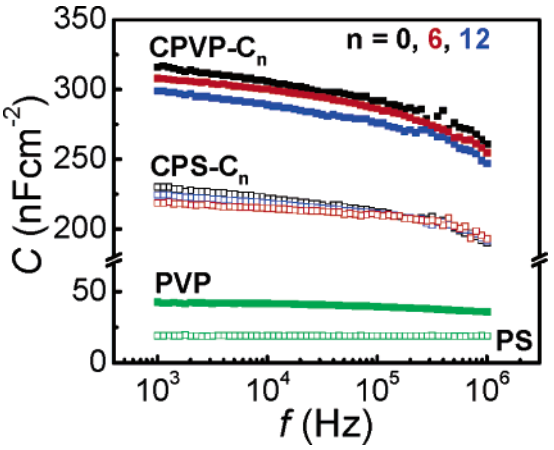

Figure 6. Capacitance-frequency plots (1−1000 kHz; film thicknesses given in Table 1) for the polymer dielectrics investigated in this study.

tor (MIS, M = Au, S = n+-Si) and metal−insulator-metal (MIM, M = ITO, Au) structures.[45] Both structures provide quantitatively similar results. Representative C_i-f plots are shown in Figure 6, with the data (Table 1) demonstrating that CPB films exhibit large capacitances [C_i (**CPVP-C$_n$**) ~ 300 nFcm^{-2}, C_i (**CPS-C$_n$**) ~ 225 nFcm^{-2}; ± 5% at 10^3 Hz], far greater than 300 nm-thick SiO_2 OTFT gate dielectrics (~10 nFcm^{-2}).[46] In contrast, the capacitance of thin **PVP** and **PS** films (<20 nm, not shown) cannot be measured due to large leakage currents, and the capacitances of ~130 nm-thick films (still too leaky for practical OTFTs; Figure 4B) are substantially lower (Table 1).

If for a variety of reasons (e.g., in nongate areas) it is desired to reduce C_i, this should be readily achieved by increasing the layer thickness. Note that CPB C_i values are reproducible and stable with time, indicating in contrast to PVP,[47] CPB polymers are minimally hygroscopic. Furthermore, samples do not exhibit appreciable variation in C_i/J characteristics over 17 months in ambient, and dielectric strength is recovered after breakdown. Breakdownfields are between 3 and 6 MV cm^{-1} (see inset Figure 4A for **CPVP-C$_6$**) depending on CPB structure and voltage scan direction. The formal dielectric constants calculated using Eq 2, are 6.1−6.5 and 2.5−2.9 (10 kHz) for **CPVP-C$_n$** and **CPS-C$_n$** films, respectively. These values are reasonable considering that the reported **PVP** and **PS** dielectric constants are ~3.6,[48] −8,[35] and ~2.5,[49] respectively—close to values independently measured in this study (6.4 and 2.6, respectively). The loss factors for the present dielectrics are also reasonably low (<0.1 at 10^4 Hz) considering that processing is not yet fully optimized. Finally, all of the CPB films exhibit little hysteresis in the C_i-V plots, suggesting that the positive fixed charge density is very low and portending good operational lifetime.[50] Typical hysteresis shifts are < 0.1 V and < 0.5 V for **CPVP-C$_n$** and **CPS-C$_n$**, respectively, and do not vary with air exposure. Exhaustive polymer purification, design/blending of different (co)polymers, and film fabrication in a dust-free environment should further enhance performance. Furthermore, dielectric constant tuning should be possible with cross-linker optimization. From the above data, **CPVP-C$_6$** is the most attractive

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Table 2. Field Effect Transistor Data for CPVP- and CPS-C_6-based Devices with Different Organic Semiconductors and Gate Substrates[a]

semicond.	dielec./subst.	μ ($cm^2V^{-1}s^{-1}$)	I_{on}:I_{off}[b]	V_T (V)	S[d] (V/dec)
1. Pentacene	CPVP−C_6/n^+-Si	0.1 (0.3)	10^4 (10^5)	−1.8 (−2.3)	0.45 (8)
2. DH-6T	CPVP−C_6/n^+-Si	0.1 (0.1)	10^3 (10^4)	0.9 (−4)	0.47
3. DHPTTP	CPVP−C_6/n^+-Si	0.01 (0.02)	10^4 (10^5)	−1.2 (−5)	0.28
4. P3HT	CPVP−C_6/n^+-Si	4×10^{-3} (5×10^{-3})	10^2 (10^3)	1.2 (20)	0.54 (9)
5. CuFPc	CPVP−C_6/n^+-Si	5×10^{-3} (3×10^{-3})	10^3 (10^4)	0.5 (20)	0.40
6. Pentacene[c]	CPVP−C_6/n^+-Si	2×10^{-3}	10^3	−0.7[c]	0.63[c]
7. Pentacene	CPS−C_6/n^+-Si	0.08	10^4	−2.0	0.35
8. Pentacene	CPVP−C_6/ITO-Glass	0.01	10^3	−0.4	0.58
9. Pentacene	CPVP−C_6/ITO-Mylar	0.06	10^4	−0.6	0.29
10. Pentacene	CPVP−C_6/Al	0.03	10^3	−0.2	0.28

[a] Data in parentheses are for 300 nm-thick SiO_2 devices with the semiconductor films grown under the same condition as for **CPVP**- and **CPS-C_6**. All TFT mobilities (μ) and threshold voltages (V_T) are calculated in the saturation regime. [b] Calculated at $V_G = 0.0 - \pm 4.0$ V ($0 - \pm 100$ V) and $V_{DS} = \pm 4.0$ V (± 100 V). [c] Data for bottom-contact configuration. [d] Subthreshold voltage swing ($S = dV_G/d(\log I_{DS})$).

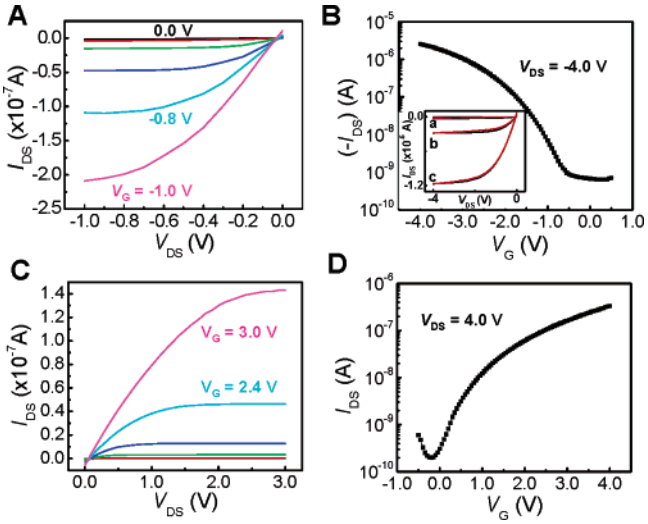

Figure 7. Performance of representative TFT devices at low biases with a cross-linked **CPVP-C_6** gate dielectric layer on an n^+-Si gate. A. Current−voltage plot as a function of V_G for **DH-6T** (p-type). B. TFT transfer plot of current vs V_G for pentacene (p-type). **Inset:** I_{DS}-V_{DS} plot as a function of V_G ($a = 0$ −2.4 V, $b = -3.2$ V, $c = -4.0$ V) showing forward (black) and reverse (red) V_{DS} scans**.** C. Current−voltage plot as a function of V_G for **CuFPc** (n-type). D. Corresponding TFT transfer plot of current vs V_G.

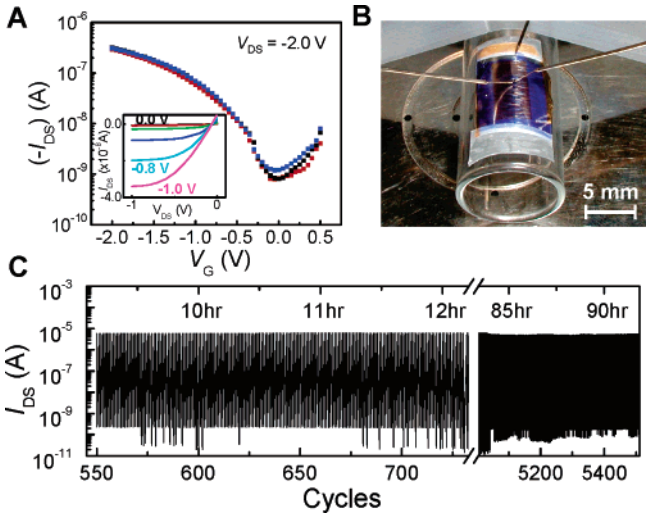

Figure 8. Pentacene TFT devices having a **CPVP−C_6** gate dielectric. A. Transfer plot of current vs V_G on an Al foil gate before bending (red), after bending 10 times (black), and after bending 30 times (blue). The measurements after bending were carried out on a bent device, with a curvature radius of 7 mm. Inset: Corresponding current−voltage plot as a function of V_G. B. Image of the device on an Al foil gate during measurement. Scale-bar denotes 3 mm. C. OTFT operational stability in air driven by square-wave pulses $V_G = 0$ V to + 2.0 V with $V_{DS} = +2.0$ V.

member of the CPB series in terms of large capacitance, low leakage currents, and smooth morphology, and so **CPVP-C_6** was examined most extensively for OTFT fabrication and evaluation.

Thin Film Transistor Fabrication and Properties. The principal TFT structures investigated utilized **CPVP-C_6** and, for comparison, **CPS-C_6**, spin-coated on the gate, followed by the semiconductor and Au source-drain contact deposition (top-contact TFT). Devices fabricated on n^+-Si substrates were used to demonstrate CPB compatibility with a variety of semiconductors, whereas pentacene OTFTs were investigated to demonstrate CPB compatibility with many gate materials in both top- and bottom-contact geometries. For semiconductor generality, a variety of molecular and polymeric p- (hole transporter) and n- (electron-transporter) channel semiconductors were selected (structures in Figure 1), with films deposited by either vapor- or solution methods. Figure 7 shows typical *I-V* plots for **DH-6T** and pentacene (vapor-deposited, p-type) and **CuFPc** (vapor-deposited, n-type). These data demonstrate that **CPVP-C_6**-based TFTs exhibit excellent linear/saturation characteristics and operate at low voltages (as low as ~ 1 V), reflecting the large capacitance and low leakage currents of the CPB gate dielectric. Typical laboratory-scale device yields approach 100%. In marked contrast, control devices fabricated with a thicker (300 nm) SiO_2 dielectric film require far larger operating voltages for a useful I_{DS}. CPB OTFT data summarized in Table 2 show that carrier mobilities are comparable to those of SiO_2-based devices fabricated under identical conditions. Moreover, the V_Ts are now only a fraction/few volts and subthreshold voltage swing (S) parameters are very low. Note that for ease of initial comparison, all semiconductor films discussed here were deposited at an identical substrate temperature (60 °C), not necessarily optimum for each semiconductor. Pentacene/**CPVP-C_6** OTFT devices achieve $\mu \approx 0.1$ cm^2 $V^{-1}s^{-1}$ versus ≈ 0.3 cm^2 $V^{-1}s^{-1}$ for those with SiO_2 dielectrics and $I_{on}/I_{off} \approx 10^4$ at $V_G = 4$ V. Bottom-contact pentacene TFTs also perform well (Table 2, entry 6). Note that devices as old as 13 months stored in air work properly, with no change in the *I-V* characteristics. Also, typical n-type semiconductors such as **CuFPc** behave similarly on **CPVP-C_6** vs SiO_2 dielectrics with $\mu \approx 0.005$ cm^2 $V^{-1}s^{-1}$ and $I_{on}/I_{off} > 10^3$ (Table 2, entry 5). Note that these TFTs show little hysteresis [$(\Delta I_{DS}/I_{DS})_{max} < 10\%$)] in $I_{DS}-V_{DS}$ plots, confirming the good quality of the dielectric material (Inset Figure 7B). Importantly, solution deposition of an additional organic layer on top does not adversely affect CPB insulator properties. Thus, TFTs fabricated with **P3HT** (spin-coated from

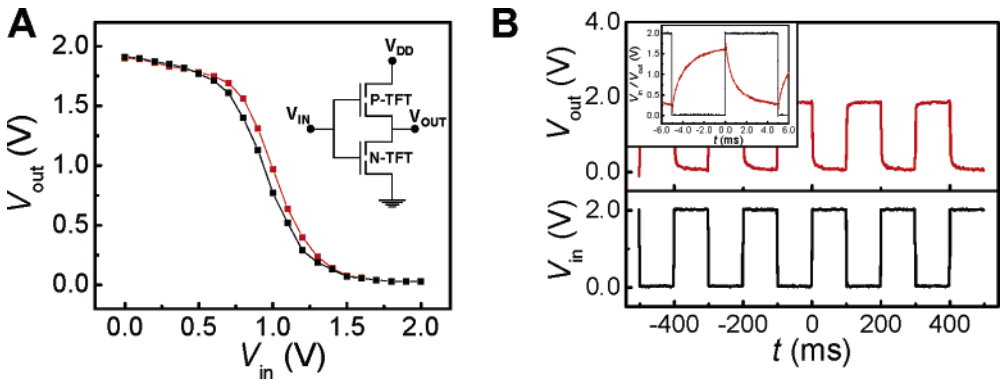

Figure 9. Performance of inverter devices. A. Complementary CPB-based inverter using a pentacene TFT ($L = 100$ μm, $W = 5$ mm) and a **CuFPc** TFT ($L = 50$ μm, $W = 5$ mm). Static characteristics measured with increasing (black) and decreasing (red) input voltage ($V_{DD} = +2.0$ V). **Inset:** Schematic electrical connections of the inverter. B. Dynamic switching characteristics of the inverter at 5 Hz. **Inset:** Dynamic switching characteristics of the inverter at 100 Hz.

$CHCl_3$) and **DH-PTTP** (solution-cast from xylene) display good transistor response characteristics at very low voltages (entries 2, 3). Pentacene TFTs having a **CPVP-C_6** gate dielectric were also fabricated on a variety of substrates, demonstrating broad versatility. Thus, TFTs on ITO/glass (entry 8), ITO/Mylar (entry 9), and kitchen Al foil (entry 10) exhibit excellent response characteristics, and the Al foil-based devices can be repeatedly bent with negligible degradation of TFT performance (Figure 8A,B). Note that these results are achieved on large device areas and unpatterned materials, and more sophisticated patterning and structure optimization should additionally improve performance and current modulation.

Finally, the remarkable stability of OTFTs fabricated with CPB gate dielectrics (when the semiconductor is itself environmentally stable) is shown in Figure 8C. Pentacene TFTs can be continuously cycled in air (relative humidity $\approx$ 80%, $T =$ 22−25 °C) between $V_G = 0$ and $+3$ V without detectable "on" current and I_{on}/I_{off} degradation over periods $>$ 100 h. This result confirms the excellent dielectric quality and that the dielectric-semiconductor interface is largely free of reactive groups that can act as charge carrier traps.

As a consequence of the CPB dielectric robustness and compatibility with both p- and n-type semiconductors, the fabrication of complementary logic devices is possible. Thus, inverters having pentacene (p-type) and **CuFPc** (n-type) transistors were fabricated with a common gate as input voltage (V_{IN}). It can be seen that they operate at very low voltages (Figure 9A). Inverter response is clearly observed for switching between logic "1" (2 V) and logic "0" (0 V) with the small hysteresis reflecting the transistor threshold voltage stability. The voltage gain $dV_{OUT}/dV_{IN} \approx 3.5$ (> 1) implies that these devices could be used to switch subsequent stages in more complex logic circuits. These inverters can be switched at frequencies up to $\sim$100 Hz, with a $\tau \approx 1.5$ ms fall time and a $\tau \approx 2.3$ ms rise time (Figure 9B). Such speeds are more than enough to operate an electrophoretic ink-based display. For more demanding applications, such as organic RF−ID tags, obvious device improvements are expected by employing higher-mobility n-type materials,[20] patterning the gate electrode (to reduce source-drain-to-gate overlap capacitance), and reducing channel length (the channel length in this proof-of-concept device is 100 μm, greater than the 5−10 μm typically used in optimized organic ICs).[6−11]

Conclusions

In summary, we have demonstrated here that blending of appropriate commercially available polymers and organosilane cross-linking agents affords robust, smooth, adherent, pinhole-free, high-capacitance, low-leakage ultrathin (10−20 nm) gate dielectric materials. These films are readily deposited from solution, adhere strongly to a variety of rigid and flexible conducting substrates, can be patterned, and are compatible with a broad range of organic semiconductors. The resulting OTFTs and complementary inverter devices function at unprecedentedly low operating voltages for a polymer-based gate dielectric and circuits speeds could be maximized via proper device design These results demonstrate that implementing these polymer dielectrics in solution-processing methodologies offers low voltage, low power operation.

Acknowledgment. We thank the NASA Institute for Nanoelectronics and Computing (NCC2-3163), ONR (N00014-02-1-0909), AFOS (STTR FA 9550-04-C-0080), and the NSF-MRSEC program through the Northwestern Materials Research Center (DMR-0076097) for support. We thank Prof. M. Hersam and L. Pingree for AFM images.

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